ABSTRACT OF THE DISCLOSURE

A fill pattern for a semiconductor device. The device includes a plurality of first topographic structures comprising conductive lead lines deposited on a semiconductor substrate, and a plurality of second topographic structures comprising fill patterns such that the top surfaces of the second topographic structures are generally coplanar with the top surfaces of the plurality of first topographic structures. The plurality of first and second topographic structures are arranged in a generally repeating array on the substrate. A planarization layer is deposited on top of the substrate such that it fills the space between the plurality of first and second topographic structures, with its top surface generally coplanar with that of the top surfaces of the first and second topographic structures.